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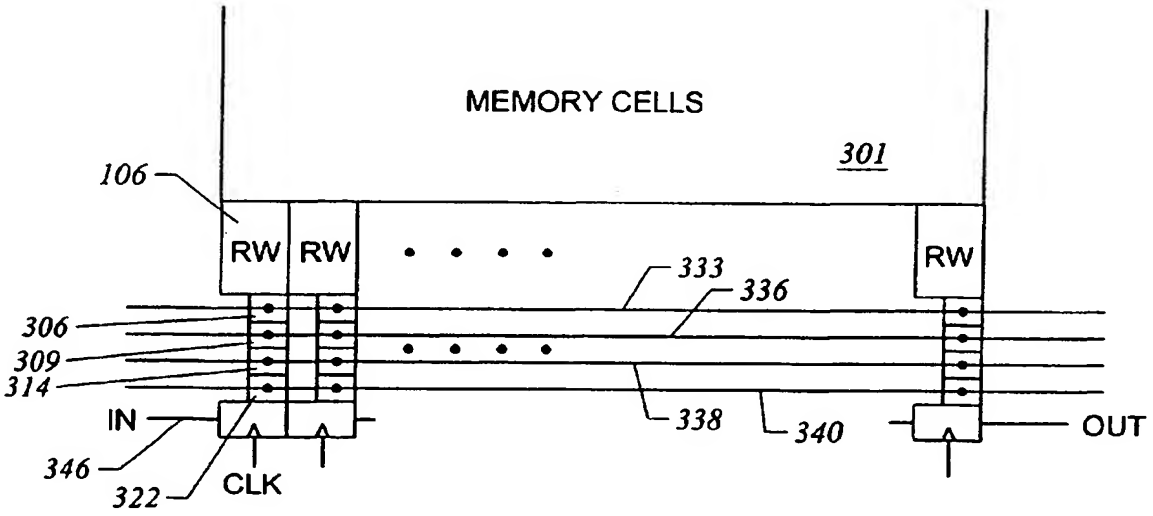

(57) Abstract: Selecting circuits for columns of an array of memory cells are used to hold read data or write data of the memory cells. The memory cells may be multistate memory cells. There is a shift register chain, having a stage for columns of the array. A strobe pulse is shifted through this shift register. The strobe points, with each clock, at and enables a different selecting circuit in sequence. That particular selecting circuit that has been enabled by the strobe will then perform a certain function. In a read mode, the selected selecting circuit will send the stored information through to the output buffer for output from the integrated circuit. And while in a programming mode, the selected selecting circuit will receive data from an input buffer. This data will be written into a memory cell.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

DYNAMIC COLUMN BLOCK SELECTION

BACKGROUND OF THE INVENTION

The present invention relates to nonvolatile erasable programmable memories and more specifically, techniques for reading and writing data for these types of memories.

Memory and storage is one of the key technology areas that is enabling the growth in the information age. With the rapid growth in the Internet, World Wide Web (WWW), wireless phones, personal digital assistant, digital cameras, digital camcorders, digital music players, computers, networks, and more, there is continually a need for better memory and storage technology. A particular type of memory is nonvolatile memory. A nonvolatile memory retains its memory or stored state even when power is removed. Some types of nonvolatile erasable programmable memories include Flash, EEPROM, EPROM, MRAM, FRAM, ferroelectric, and magnetic memories. Some nonvolatile storage products include CompactFlash (CF) cards, MultiMedia cards (MMC), Flash PC cards (*e.g.*, ATA Flash cards), SmartMedia cards, and memory sticks.

A widely used type of semiconductor memory storage cell is the floating gate memory cell. Some types of floating gate memory cells include Flash, EEPROM, and EPROM. The memory cells are configured or programmed to a desired configured state. In particular, electric charge is placed on or removed from the floating gate of a Flash memory cell to put the memory into two or more stored states. One state is an erased state and there may be one or more programmed states. Alternatively, depending on the technology and terminology, there may be a programmed state and one or more erased states. A Flash memory cell can be used to represent at least two binary states, a 0 or a 1. A Flash memory cell can store more than two binary states, such as a 00, 01, 10, or 11; this cell can store multiple states and may be referred to as a multistate memory cell. The cell may have more than one programmed states. If one state is the erased state (00), the programmed states will be 01, 10, and 11, although the actual encoding of the states may vary.

Despite the success of nonvolatile memories, there also continues to be a need to improve the technology. It is desirable to improve the density, speed, durability, and reliability of these memories. It is also desirable to reduce power consumption.

As can be seen, there is a need for improving the operation of nonvolatile memories. Specifically, by using a technique of dynamic column block selection of the memory cells, this will reduce noise in the operation of the integrated circuit, which will permit the integrated circuit to operate more reliably. Further, the technique will also reduce the area required by the block selection circuitry, which will reduce the cost of manufacture.

SUMMARY OF THE INVENTION

The invention provides a technique of accessing selecting circuits assigned to columns of an array of memory cells to hold data read or to be written into the memory cells. The selecting circuits may be latches. In a specific embodiment, the memory cells are multistate memory cells. There is a shift register, acting as a pointer, having a stage for each column block of the array. A strobe pulse is shifted through this shift register. The strobe points, with each clock, at and enables a different circuit in sequence. That particular selecting circuit that has been enabled by the strobe will then perform a certain operation. In a read mode, the selected selecting circuit will transfer the stored information through an output line to the output buffer for output from the integrated circuit. And while in a programming mode, the selected selecting circuit will receive data from an input buffer. This data will be written into a memory cell.

In one specific embodiment, the invention is an integrated circuit including a number of nonvolatile memory cells arranged in rows and columns. A number of read/write circuits are connected to a number of array columns of memory cells. In an embodiment, a read/write circuit includes a sense amplifier circuit. A number of first latch circuits are connected to the same set of read/write circuits and a first I/O line. A number of second latch circuits are connected to one or more sense amplifiers and a second I/O line. There is a shift register chain including a number of shift register stages, acting as pointers. Each stage has a data input and a data output. Each stage has a clock input. Each shift register has its input connected to the previous shift register output and the output connected to the next shift register input.

Accordingly, those cells are floating gate devices. Flash, EEPROM, or EPROM memory cells are some examples of floating gate devices. The first latches may be implemented

using a pair of cross-coupled inverters. The second latches may be implemented using a pair of cross-coupled inverters. Other techniques for implementing a latch may be used such as using other logic gates including NAND and NOR. Each stage of the shift register may be a master-slave-type register. Each memory cell may store a plurality of bits of data. The memory cells may be multistate memory cells. One of the first latch circuits and one of the second latch circuits may hold data to be written into or read from a single memory cell for a column of the memory cells. The first latches are connected between the first I/O line and a different one of the read/write circuits. Furthermore, the second latches are connected between the second I/O line and the same read/write circuit as the first latch one of the sense amplifiers.

The first and second latches are not part of a shift register. The first latch circuits do not form a shift register. The second latch circuits do not form a shift register. Therefore, data is not serially passed from one of the first latch circuits to a next one of the first latch circuits. Data is not serially passed from one of the second latch circuits to a next one of the second latch circuits.

In another embodiment, the invention is a method of operating an integrated circuit. A first latch is provided to hold data associated with a first column of memory cells. A second latch is provided to hold data associated with a second column of memory cells. A shift register is provided having a first stage with an output connected to an enable input of the first latch, and a second stage with an output connected to an enable input of the second latch. A strobe bit is loaded into the first stage of the shift register to enable connecting of the first latch to an I/O line. The shift register is clocked to advance the strobe bit from the first stage of the shift register to the second stage to enable connecting of the second latch to the I/O line. Connecting of the first latch to the I/O line is disabled upon clocking the shift register.

Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows an integrated circuit with shift registers for holding data to be read and written into the memory.

Figure 2 shows an implementation of a master-slave register.

Figure 3 shows an integrated circuit with latches for holding data to be read and written into the memory.

Figure 4 shows an implementation of a latch.

Figure 5 shows connecting a first data latch to an I/O line by placing a 1 in a first stage of a shift register.

Figure 6 shows connecting a second data latch to the I/O line by placing a 1 in a second stage of a shift register.

Figure 7 shows an embodiment of the invention with multiple input lines and a single output line.

Figure 8 shows an embodiment of the invention with a single input line and a single output line.

DETAILED DESCRIPTION

Integrated circuits providing nonvolatile storage include nonvolatile erasable-programmable memory cells. Many types of integrated circuits having nonvolatile memory cells include memories, microcontrollers, microprocessors, and programmable logic. Nonvolatile memory integrated circuits may be combined with other nonvolatile memory integrated circuits to form larger memories. The nonvolatile memory integrated circuits may also be combined with other integrated circuits or components such as controllers, microprocessors, random access memories (RAM), or I/O devices, to form a nonvolatile memory system. An example of a Flash EEPROM system is discussed in U.S. patent 5,602,987, which is incorporated by reference along with all references cited in this application.

Further discussion of nonvolatile cells and storage is in U.S. patents 5,095,344, 5,270,979, 5,380,672, 5,712,180, 6,222,762, and 6,230,233, which are incorporated by reference.

Some types of nonvolatile storage or memory cells include Flash, EEPROM, and EPROM. There are many other types of nonvolatile memory technologies and the present invention may be applied to these technologies as well as other technologies. Some examples of other nonvolatile technologies include MRAM and FRAM cells. This patent application discusses some specific embodiments of the invention as applied to Flash or EEPROM technology. However, this discussion is to provide merely an specific example of an application of the invention and is not intended to limit the invention to Flash or EEPROM technology.

Figure 1 shows a memory integrated circuit with memory cells 101. The integrated circuit may be a memory such as a Flash chip or may be an integrated circuit with a embedded memory portion, such as an ASIC or microprocessor with memory. The memory cells store binary information. In a specific embodiment, the memory cells are nonvolatile memory cells. Examples of some nonvolatile memory cells are floating gate cells, which include Flash, EEPROM, or EPROM cells. The memory cells are arranged in an array of rows and columns. There may be any number of rows and columns. read/write circuit 106 are coupled to columns of the memory cells. In an embodiment, there is one read/write circuit for each column of memory cells. In other embodiments, one read/write circuit may be shared among two or more columns of memory cells. Sense amplifiers are used to read the states of the memory cells. The sense amplifies may also be combined with other circuits in order to write or store data into the memory cells. The combination is referred to as a read/write circuit.

In a specific embodiment, the memory cells are multistate cells, capable of storing multiple bits of data per cell. In Figure 1, the memory cells store two bits of data. This dual-bit memory cell was selected in order to illustrate the principles of the invention. Multistate memory cells may store more than two bits of data, such as three, four, and more.

Figure 1 shows four shift registers 109, 114, 117, and 122. Each shift register stage has an input of IN and an output or OUT. Data is clocked in and out of the registers using a clock input at a CLK input. The clock input is connected to all the registers.

An example of a specific circuit implementation of a register of the shift register is shown in Figure 2. This is known as a master-slave register. There are other circuit implementations for a register that may be used. An input 202 is the input to the shift register or is connected to a previous stage of the shift register. An output 206 is the output to the shift register or is connected to a next stage of the shift register.

Each of the four shift registers has one register which is associated with and connected to a particular read-write (RW) circuit. Each read-write circuit includes circuitry to read a state of memory cell and circuitry to write data into a memory cell. The circuitry was shown as a single block, but could also be drawn as two blocks, one for the write circuitry and one for the read circuitry. An example of read circuitry is a sense amplifier (SA) circuit. In other words, each read-write circuit has four registers associated with it. Two of these registers are used to hold the data to be written into the memory cell. Two registers are used to load the

new data to be written while programming is is proceeding, for improved performance. For example, registers 109 and 114 may be used to hold write data, and registers 117 and 122 may be used to load write data. The write data is serially streamed into the shift registers using IN and then written using read-write circuitry (*i.e.*, write circuit) into the memory cells. Data from the memory cells is read out using the read-write circuit (*i.e.*, read circuit or sense amplifier) and stored into the registers. The sense amplifiers can sense in parallel and dump data in parallel, in the shift registers.

For memory cells that hold more than two bits per cell, there would be an additional register for each additional bit. For example, for three bits per cell, there would be an additional two shift registers. Three registers for read data, and three registers for write data.

The embodiment of Figure 1 shows a separate set of registers for loading/unloading and actual read and write data. In other embodiments, one set of registers may be shared to handle both load and write or read and unload; this will save integrated circuit area. However, by having individual sets of registers for load and write or read and unload, this improves performance because both types of operation can occur at the same time. Furthermore, in an alternative embodiment, there may be separate clocks, such as a read clock and a write clock, for the read and write registers. This will allow independent inputting of data into the respective read or write data shift register.

As bits are clocked into and out of the shift registers, depending on the particular pattern of the data, there may be a significant amount of switching noise. For example, if the pattern were a string of alternating 0s and 1s (*i.e.*, 01010101 . . . 0101), this would generate a lot of switching noise because there will be full rail transitions occurring at each clock. And the noise if further dependent on the number of shift registers switching at the same time.

In summary for the approach in Figure 1, the circuits store and transfer data by means of shift registers: In read mode, read circuitry or sense amplifiers dump data into shift registers, then data are streamed out. During programming, data are shifted in and stored into these shift registers. Shift registers are made of two latches, a "master" and a "slave." Shifting in or out data through the masters and the slaves creates a lot of noise, depending upon data pattern. For example, if data is mostly alternating 0s and 1s, then thousand of masters and slaves will toggle their outputs accordingly.

Figure 3 shows another circuit architecture for reading and writing data to memory cells 301 of an integrated circuit. This architecture requires less integrated circuit area and generates less noise than that in Figure 1, especially for high density, multistate memory cells. The integrated circuit may be a memory such as a Flash chip or may be an integrated circuit with a embedded memory portion, such as an ASIC or microprocessor with memory. The memory cells store binary information. In a specific embodiment, the memory cells are nonvolatile memory cells. Examples of some nonvolatile memory cells are floating gate, Flash, or EEPROM cells. The memory cells are arranged in an array of rows and columns. The may be any number of rows and columns.

Read-write (RW) circuits 306 are coupled to columns of the memory cells. In an embodiment, there is one read-write circuit for each column of memory cells. In other embodiments, one read-write circuit may be shared among two or more columns of memory cells. The read-write circuits are used to read the states of the memory cells. The read-write circuits may be also be used to write or store data into the memory cells. The read-write circuitry may include sense amplifier circuits, as discussed above.

In a specific embodiment, the memory cells are multistate cells, capable of storing multiple bits of data per cell. As with the embodiment of Figure 1, for the purpose of serving as an exemplary embodiment, memory cells 301 of Figure 3 are dual-bit multibit memory cells. This dual-bit memory cell was selected in order to illustrate the principles of the invention. Multistate memory cells may store more than two bits of data, such as three, four, and more. And, the principles of the invention would also apply. As the number of bits that can be stored in a single multistate cell increases, the advantages of the architecture in Figure 3 over that in Figure 1 also increase.

There are temporary storage circuits or four data latches 306, 309, 314, and 322 associated with and connected to each read-write circuit. The temporary storage circuits may be any circuitry used to hold data for the memory cells. In a specific implementation, the temporary storage circuits are latches. However, other types of logic may also be used. The connection is not shown. Each latch is connected to one of four input lines, 333, 336, 338, and 340. These input lines are lines used to input data into the latches. Data is loaded into a particular latch based on an ENABLE signal input of each latch (not shown). When the LOAD signal is asserted (active low or active high signal) for a particular latch, then that latch is loaded.

In the figure, the input lines are shown running on top of the latches. They may also run beside the latches. Also, in other embodiments of the invention, there may be a single input line and data from the input line is shifted into the latches serially.

An example of a specific circuit implementation of a latch is shown in Figure 4. Other circuit implementation for a latch that may also be used. An input 402 is the input of the latch and will be connected to an input line. The ENABLE signal is connected to a pass transistor or pass gate that allows data to be connected to or disconnected from input 402. This latch circuit includes cross-coupled inverters to hold data. The latch also connects to the read-write circuit so that data may be passed between the circuits (such as by using pass transistor 408). The latch also connects to the output through a pass transistor 413. There are other possible implementations. For example, an input/output (I/O) line may be used, so only one of the pass transistors 402 or 413 is needed. The single pass transistor would connect the latch to the I/O line. Further, instead of inverters, other logic gates may be used, such as NAND, NOR, XOR, AND, and OR gates, and combinations of these.

Note that this circuitry contains half the circuitry of a master-slave register as shown in Figure 2. The master portion of a master-slaver register is one latch, and the slave portion is another latch.

Also, the implementation shows an NMOS or n-channel pass transistor. There are many ways to form a pass gate, and any of these techniques may be used. For example, a CMOS pass gate may be used. A CMOS pass gate includes NMOS and PMOS transistors connected in parallel. Also, a high voltage pass gate may be used. For example, a high-voltage NMOS pass gate is enabled or turned on (or placed in an on state) by placing a high voltage, above VCC, at its gate or control electrode. An NMOS pass gate are turned off or put in an off state by placing its control electrode at VSS or ground.

The circuitry in Figure 3 further includes a shift register 346, one stage for each read-write circuit. This shift register is similar to one shift register of Figure 1. The output of each shift register stage is connected to the ENABLE signal input of the particular latches that stage is associated with.

In this particular embodiment, each read-write circuit is connected to and has four latches associated with it. Two of these latches are used to hold the data to be written into the memory cell. Two latches are used to load the data to be written into the memory cell during the

next write cycle. For example, latches 309 and 314 may be used to hold write data, and latches 317 and 322 may be used to hold load new data. Accordingly, during the read mode, two latches are used to hold and unload current data, while new data is prepared in the other two latches.

The write data is input into the latches via the appropriate input lines and then written using the appropriate read-write circuit into the memory cells. Data from the memory cells is read out using the sense amplifier and stored into the latches. The read data is output from the latches using the appropriate output lines. The communication line between the latch and the read-write circuit as well as the output line is not shown.

Data is input from the latches one at a time using the input lines. This is done by using an ENABLE signal, so that the latches associated with a read-write circuit or column in the array are connected to the input lines one at a time. The ENABLE signal for a the latches comes from the shift registers. The shift registers are loaded with a pattern (for active high logic) which is all 0s, except for one 1 (*e.g.*, 0001000000). This bit may be referred to as a strobe bit. For example, shift register associated with the first column has a 1, and the rest of the shift register contain 0. This 1 is connected to the ENABLE input of the latches for the first column, which connects one or more of these latches to the I/O lines 333, 336, 338, and 340. Data can be read or written to this column. The input to the shift register is connected to 0 and the shift register is clocked. The 1 propagates to the next shift register stage. This 1 is connected to the ENABLE input of the latches for the second column, which connects these latches to the I/O lines. This operation continues until the desired data is read or written from the latches.

Figures 5 and 6 show more clearly the operation of latches and shift register. In Figure 5, the first shift register has a 1; the data latch associated with that shift register and column is connected to the I/O line. In Figure 6, the shift register has been clocked, and the next shift register has the 1; the data latch associated with that shift register and column is connected to the I/O line.

The circuitry may also be designed for an active low LOAD signal. Then, the shift register will contain all 1s and a 0 for the particular latches to be enabled (*e.g.*, 1110111111).

For multistate (or multibit) memory cells that hold more than two bits per cell, there would be an additional latch for each additional bit. For example, for three bits per cell, there would be an additional two latches. Three latches for outputting data, and three latches for

preparing data, or three to write, three to input new data for the next cycle. Only one shift register is required to provide an enable signal.

The embodiment of Figure 3 shows a separate set of latches for shifting in or out (loading/unloading) data and the actual operation. In other embodiments, one set of latches may be shared to handle serially the shifting and this will save integrated circuit area. However, by having individual sets of registers for read and write, this improves performance because both types of data may be input and output at the same time.

Compared to Figure 1, the circuitry in Figure 3 requires less integrated circuit area to obtain the same functionality. And, the integrated circuit area savings increases as the number of bits stored per memory cell increases. This is because a latch takes up about half the area as a master-slave register. For Figure 1, the number of latches used per column is given by A=d*4 per column, where d is the number of bits stored in a single memory cell. For Figure 3, the number of latches used per column is given by B=d*2+2. The table below summarizes the integrated circuit area savings by number of latches. As can be seen, as d increases, the integrated circuit area savings of approach B over approach A increases. And, there may be further integrated circuit area savings depending on the number of columns.

Table

d Number of Bits per Cell	A Number of Latches Using Shift Registers	B Number of Latches Using Dynamic Column Block Selection
2	8	6
3	12	8
4	16	10
5	20	12
6	24	14
7	28	16
8	32	18

Another advantage of the Figure 3 approach over that in Figure 1 is a reduction in the amount of noise generated. When propagating a 1 (or 0 for active low) through the shift register to enable one set of latches, only one bit is being switched for each clock. Furthermore, only one set of latches is being connected to the I/O lines at a time. Both these contribute to reduce the amount of noise when inputting and output data from the memory cells. By reducing the amount of noise, this improves the reliability of the integrated circuit since it will be less like that data will be corrupted by noise.

In summary for the approach in Figure 3, data are stored in latches instead of shift registers. In addition to the data latches, there is one chain of master-slave shift registers. A strobe pulse is shifted through these registers and points, with each clock, at a different latch, in sequence. That particular latch will be then connected to an input or an output line. So, in read, the selected latch will send the stored information to the output buffer, and while in programming, the selected latch will receive data from an input buffer.

Starting with two bits per cell, area can be saved with the approach of Figure 3. In the approach of Figure 1, a set of four master-slave shift registers, or eight latches, is used. Two set/reset registers (four latches) are used to store read or programming data, and two set/reset registers (another four latches) are used to shift in data during stream write, which provides for increased performance.

With the approach of Figure 3, only six latches are necessary: Two latches (shift register) are for the shifting the strobe. Two latches are for storing old data, and two latches are for loading new data.

Furthermore, the circuitry of Figure 3 is comparatively very quiet: one clock signal and one latch output switching (for the strobe) plus two I/Os to be driven, compared to six clocks and thousands of latches switching at a time.

There are many possible embodiments of the present invention. One embodiment may use a combined input/output (I/O) line to input and output data to the latches. There may be one I/O line for each latch or there may be one I/O line for two or more latches. For example, there may be one I/O line that is shared by four latches. Or there may be four I/O lines and four latches.

Figure 7 shows the details of another embodiment of the invention. There are four input lines 333, 336, 338, and 340 for four latches 306, 309, 314, and 322, respectively.

There is a single output line 711. When a particular column of latches is enabled using the ENABLE signal from the shift register, the data on an input line is connected to and stored in a respective latch. This data in the latches may be connected to the read-write circuit 106 for writing the data into the memory cells.

This implementation includes a single output line where data from the latches are output. Another embodiment may have four output lines, one for each of the latches. However, having more lines does impact die size, and having fewer lines produces a more compact layout.

Figure 8 shows another embodiment of the invention. There is a single input line 808 that is shared by the four latches 306, 309, 314, and 322. The data from the input line may be transferred to each latch. Compared to the Figure 7 implementation, because there is a single input line in Figure 8, this implementation provides for a more compact layout.

As illustrated by these specific embodiments, there is a multitude of permutations of the present invention. For example, there may be a single I/O line for two or more latches. There may be a single I/O line for each latch. There may be one input line for two or more latches. There may be a single input line for each latch. There may be one output line for two or more latches. There may be a single output line for each latch. And each of these embodiments may be combined with others. For example, there may be one output line and one input line. There may be one input line and four output lines.

This description of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and many modifications and variations are possible in light of the teaching above. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications. This description will enable others skilled in the art to best utilize and practice the invention in various embodiments and with various modifications as are suited to a particular use. The scope of the invention is defined by the following claims.

WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a plurality of nonvolatile memory cells arranged in rows and columns;

a plurality of programming circuits coupled to the columns of memory cells;

a plurality of sense amplifiers coupled to the columns of memory cells;

a plurality of latch circuits able to temporarily store data, coupled to either the programming or sensing circuits, or to both;

a plurality of input circuits coupled to the data storage elements;

a plurality of output circuits coupled to the data storage elements; and

a pointer shift register comprising a plurality of pointer shift register stages, wherein each stage has a clock input and is coupled to an enable stage of either one or some of the programming, sensing, data storage, input and/or output circuits.

2. The integrated circuit of claim 1 wherein the memory cells are floating gate, Flash, EEPROM, or EPROM memory cells.

3. The integrated circuit of claim 1 wherein the first latch comprises a pair of cross-coupled logic gates.

4. The integrated circuit of claim 1 wherein the second latch comprises a pair of cross-coupled inverters.

5. The integrated circuit of claim 1 wherein each stage of the shift register comprises a master-slave register.

6. The integrated circuit of claim 1 wherein each memory cell stores a plurality of bits of data.

7. The integrated circuit of claim 1 wherein each memory cell stores at least one bit of information.

8. The integrated circuit of claim 1 wherein the memory cells are two state memory cells.

9. The integrated circuit of claim 1 wherein the memory cells are multistate memory cells.

10. The integrated circuit of claim 1 wherein either one of the latch circuits can temporarily store one bit of information.

11. The integrated circuit of claim 1 wherein combinations of multiple latch circuits can be assigned to store multiple bits of information.

12. The integrated circuit of claim 1 wherein each stage of the clocked pointer shift register stages can couple an input circuit to any or part of the latch circuits of claim 10.

13. The integrated circuit of claim 1 wherein each stage of the clocked pointer shift register can couple an input circuit to any or part of the latch circuits of claim11.

14. The integrated circuit of claim 1 wherein each stage of the clocked pointer shift register stages can couple an output circuit to any or part of the latch circuits of claim 10.

15. The integrated circuit of claim 1 wherein each stage of the clocked pointer shift register stages can couple an input circuit to any or part of the latch circuits of claim 11.

16. The integrated circuit of claim 1 wherein one of the first latch circuits and one of the second latch circuits hold data to be written into a single memory cell for a column of the memory cells.

17. The integrated circuit of claim 1 wherein one of the first latch circuits and one of the second latch circuits hold data read from a single memory cell for a column of the memory cells.

18. The integrated circuit of claim 1 wherein the first latches are coupled in parallel, each between the first input line and a different one of the sense amplifiers.

19. The integrated circuit of claim 1 wherein the second latches are coupled in parallel, each between a second input line and a different one of the sense amplifiers.

20. The integrated circuit of claim 1 wherein data is not serially passed from one of the first latch circuits to a next one of the first latch circuits in a different column.

21. The integrated circuit of claim 1 wherein the first latch circuits do not form a shift register.

22. A method of operating an integrated circuit comprising:

providing a first latch to hold data associated with a first column of memory cells;

providing a second latch to hold data associated with a second column of memory cells;

providing a shift register having a first stage with an output coupled to an enable input of the first latch and a second stage with an output coupled to an enable input of the second latch;

loading a strobe bit into the first stage of the shift register to enable coupling of the first latch to an input line; and

clocking the shift register to advance the strobe bit from the first stage of the shift register to the second stage to enable coupling of the second latch to the input line.

23. The method of claim 22 wherein each of the memory cells stores a plurality of bits of data.

24. The method of claim 22 wherein the memory cells are multistate memory cells.

25. The method of claim 22 further comprising:

disabling coupling of the first latch to the I/O line upon clocking the shift register.

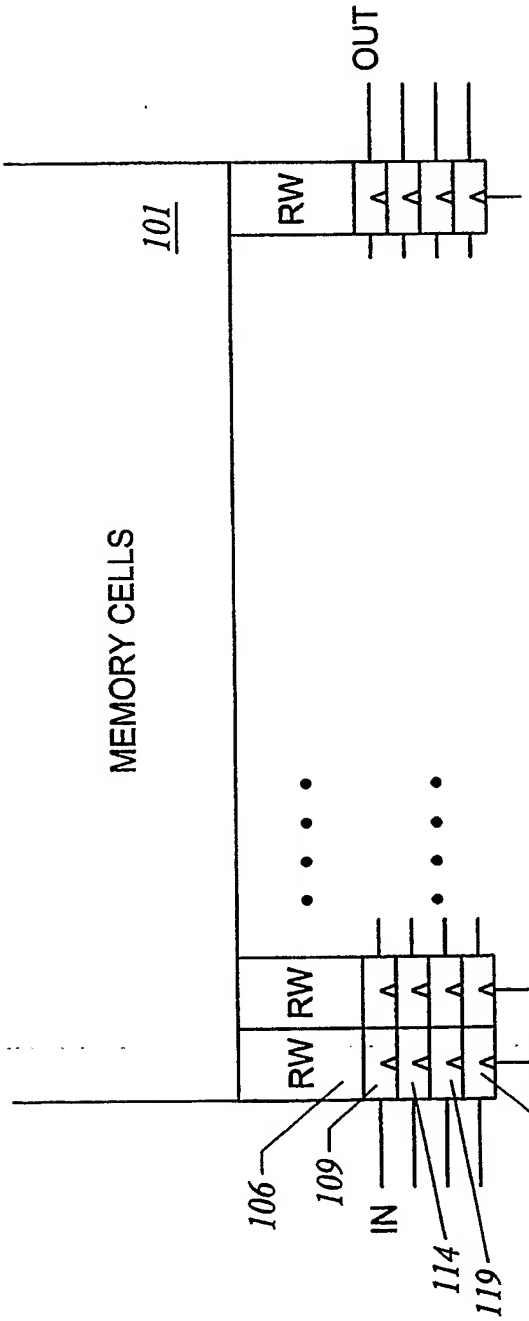
OUT
101
RW
MEMORY CELLS
RW
RW
CLK
106
109
IN
114
119
122

FIG. 1

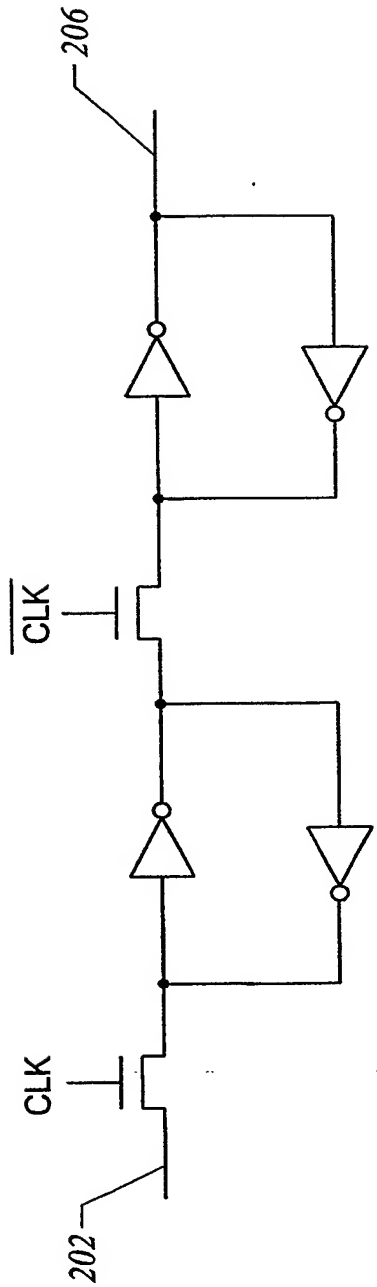
206
CLK
CLK
202

FIG. 2

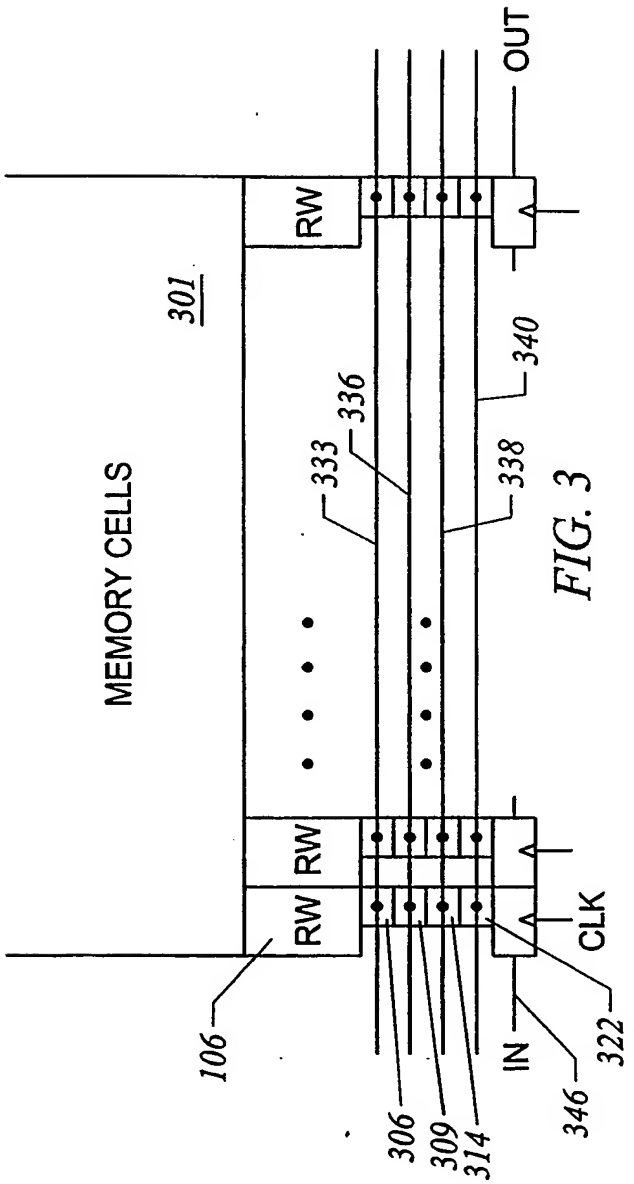

FIG. 3

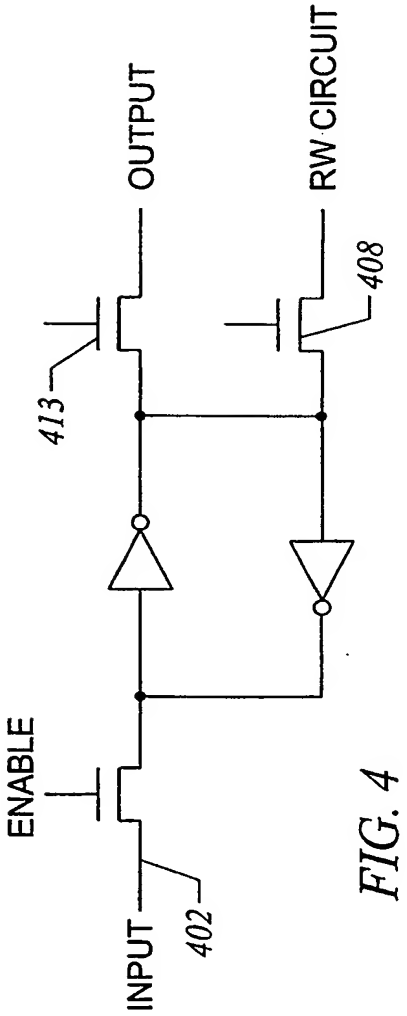

FIG. 4

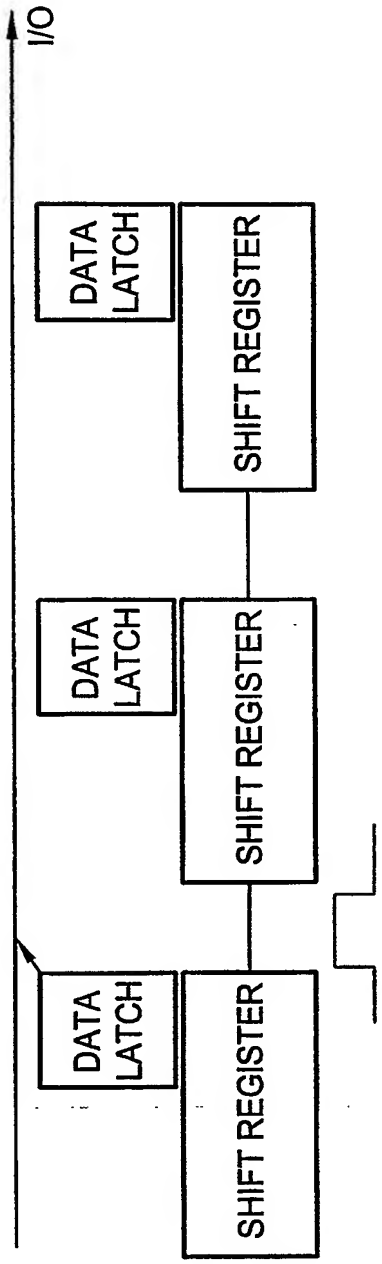

FIG. 5

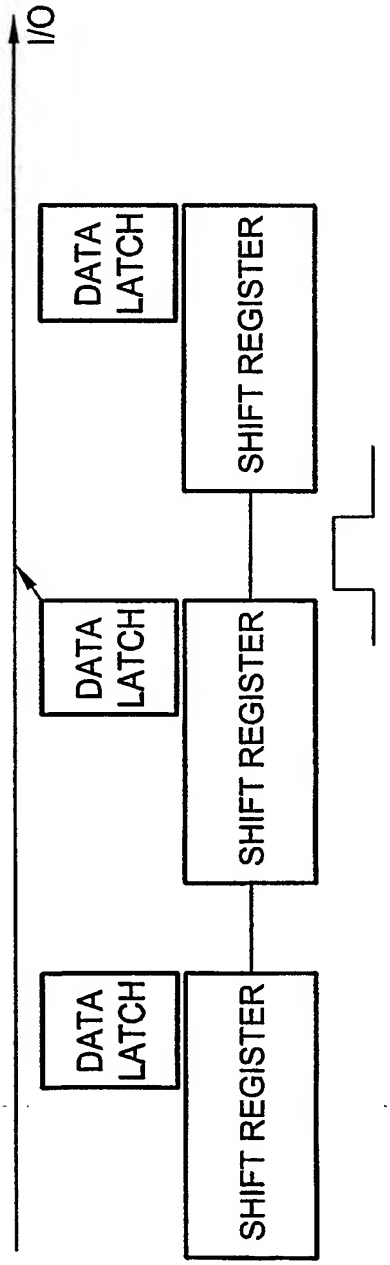

FIG. 6

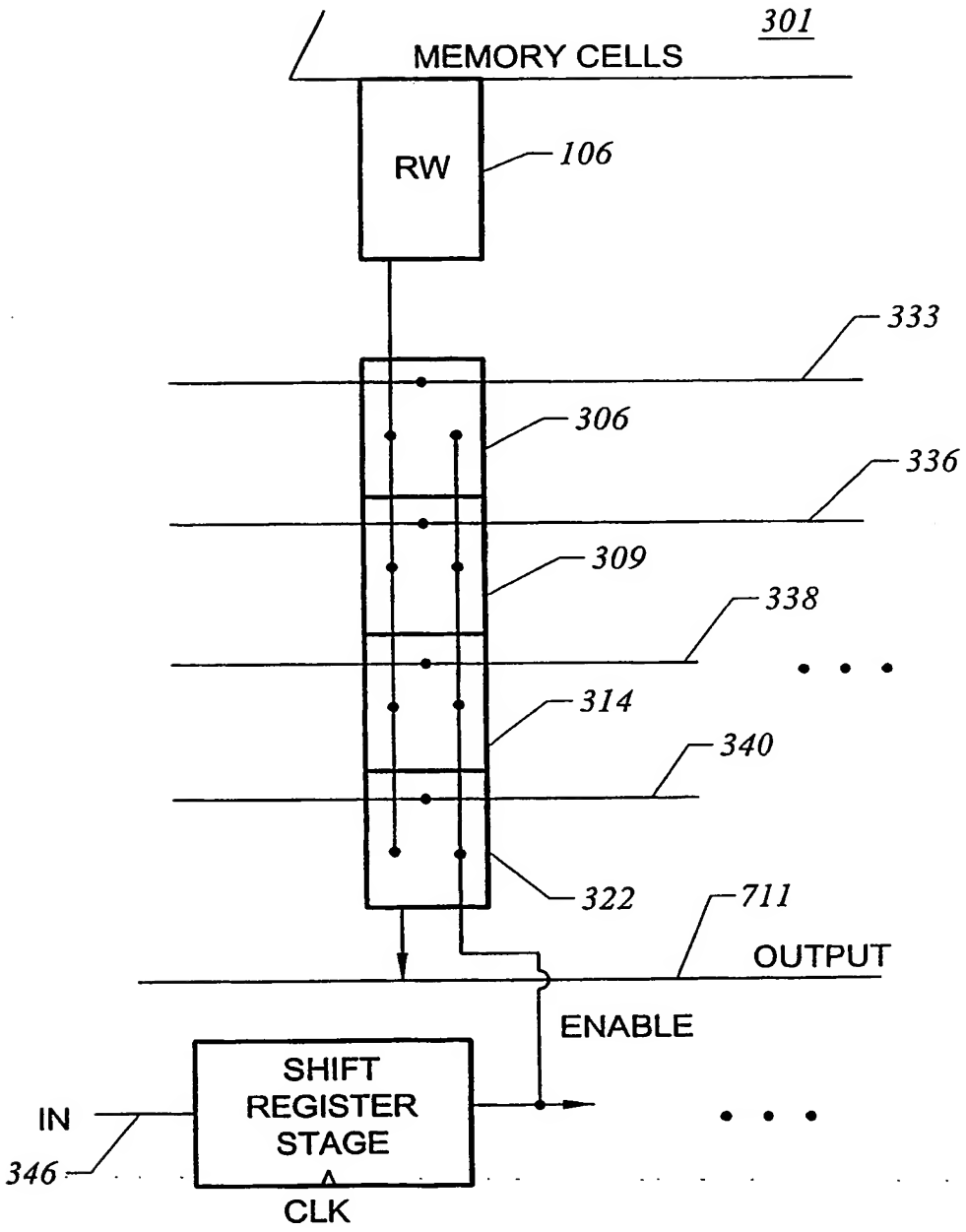

FIG. 7

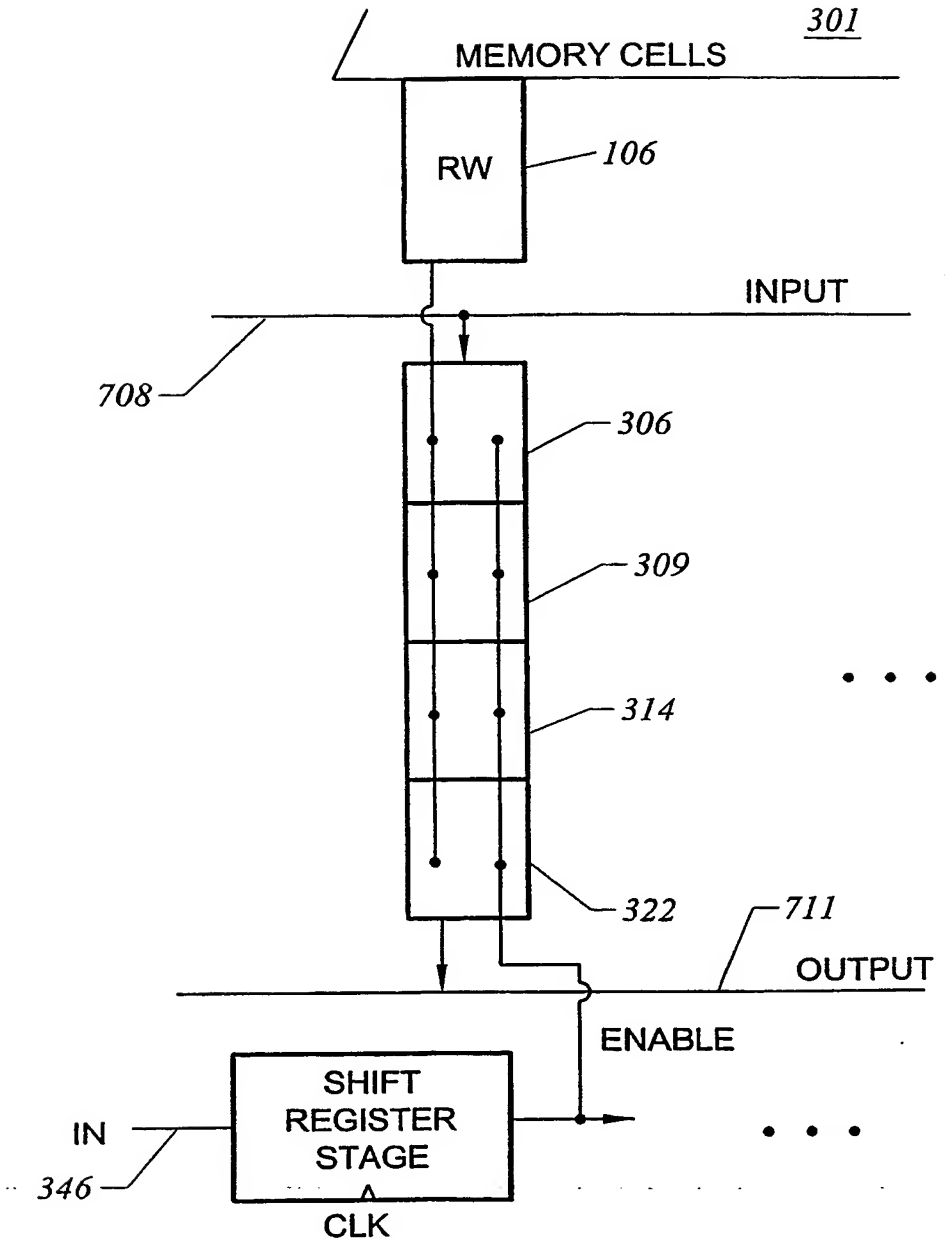

FIG. 8

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(74) Agent: **PARSONS, Gerald, P.**; Parsons Hsue & De Runtz LLP, 655 Montgomery Street, Suite 1800, San Francisco, CA 94111 (US).

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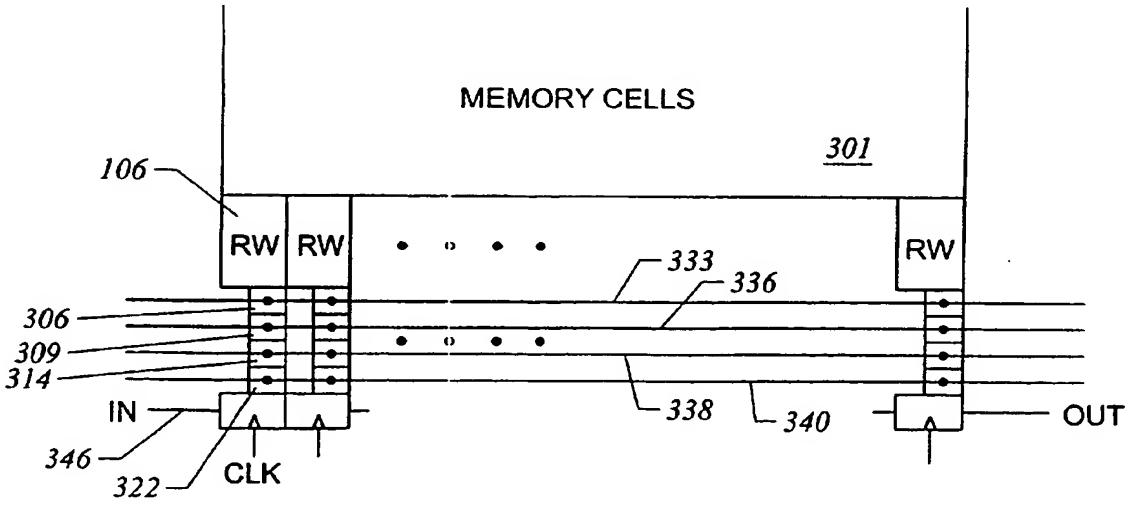
(54) Title: DYNAMIC COLUMN BLOCK SELECTION



(57) Abstract: Selecting circuits for columns of an array of memory cells are used to hold read data or write data of the memory cells. The memory cells may be multistate memory cells. There is a shift register chain, having a stage for columns of the array. A strobe pulse is shifted through this shift register. The strobe points, with each clock, at and enables a different selecting circuit in sequence. That particular selecting circuit that has been enabled by the strobe will then perform a certain function. In a read mode, the selected selecting circuit will send the stored information through to the output buffer for output from the integrated circuit. And while in a programming mode, the selected selecting circuit will receive data from an input buffer. This data will be written into a memory cell.

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INTERNATIONAL SEARCH REPORT

Ir nal Application No
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 757 477 A (BABA FUMIO ET AL) 12 July 1988 (1988-07-12) column 2, line 57 -column 3, line 61; figure 1	1-18, 20-25
X	US 4 720 815 A (OGAWA JUNJI) 19 January 1988 (1988-01-19) column 5, line 64 -column 6, line 4; figure 6	22-25
A		1-21
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Date of the actual completion of the international search	Date of mailing of the international search report
24 September 2003	02/10/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gaertner, W

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